ABSTRACT OF THE DISCLOSURE

The present invention provides a novel semiconductor integrated circuit device equipped with memory circuits, high-speed memories and large memory capacity memory circuits, which enables speeding up and facilitation of timing settings. The semiconductor integrated circuit device is provided with first amplifier circuits; which include first MOSFETs of first conductivity type, which have gates provided for a plurality of bit lines to which memory cells are respectively connected, and which are respectively maintained in an off state under precharge voltages supplied to the bit lines, as read circuits of the memory cells determined as to whether memory currents flow according to the operation of selecting word lines and memory information; and which are respectively brought to operating states in association with select signals for the bit lines, and also provided with a second amplifier circuit including; a plurality of second MOSFETs of second conductivity type, which have gates respectively supplied with a plurality of amplified signals of the first amplifier circuits and which are connected in parallel configurations; and which forms an amplified signal corresponding to the amplified signals of the first amplifier circuits.